

# Save Money by Investing In Models; Failing Early is More affordable Than Failing Late

by *Gerrit Muller* University of South-Eastern Norway-NISE

e-mail: `gaudisite@gmail.com`

`www.gaudisite.nl`

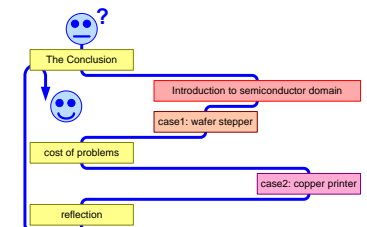
## Abstract

Many stakeholders in systems development are unaware of the unknowns. Making and using virtual and physical models helps to validate assumptions, to calibrate the understanding, and to identify uncertainties and unknowns. A major risk is that some stakeholders think that they can afford to skip the laborious phase of trial, error, trouble shoot, and validation. It is an old wisdom that it is less costly to fail early than to fail late. We will use two cases from the semiconductor industry for illustration.

### Distribution

This article or presentation is written as part of the Gaudí project. The Gaudí project philosophy is to improve by obtaining frequent feedback. Frequent feedback is pursued by an open creation process. This document is published as intermediate or nearly mature version to get feedback. Further distribution is allowed as long as the document remains complete and unchanged.

August 20, 2025  
status: preliminary  
draft  
version: 0.1

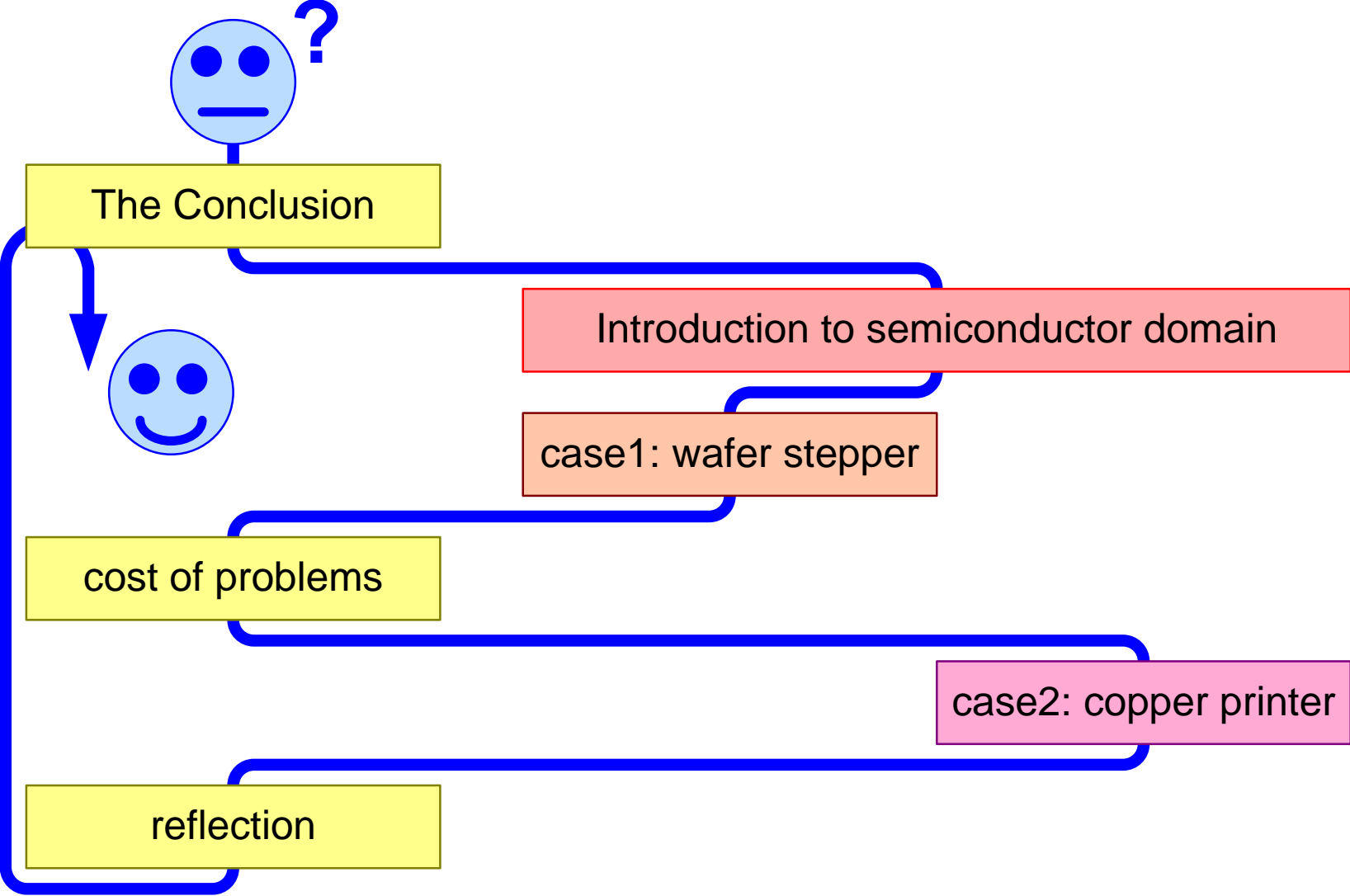


Early *investments* in

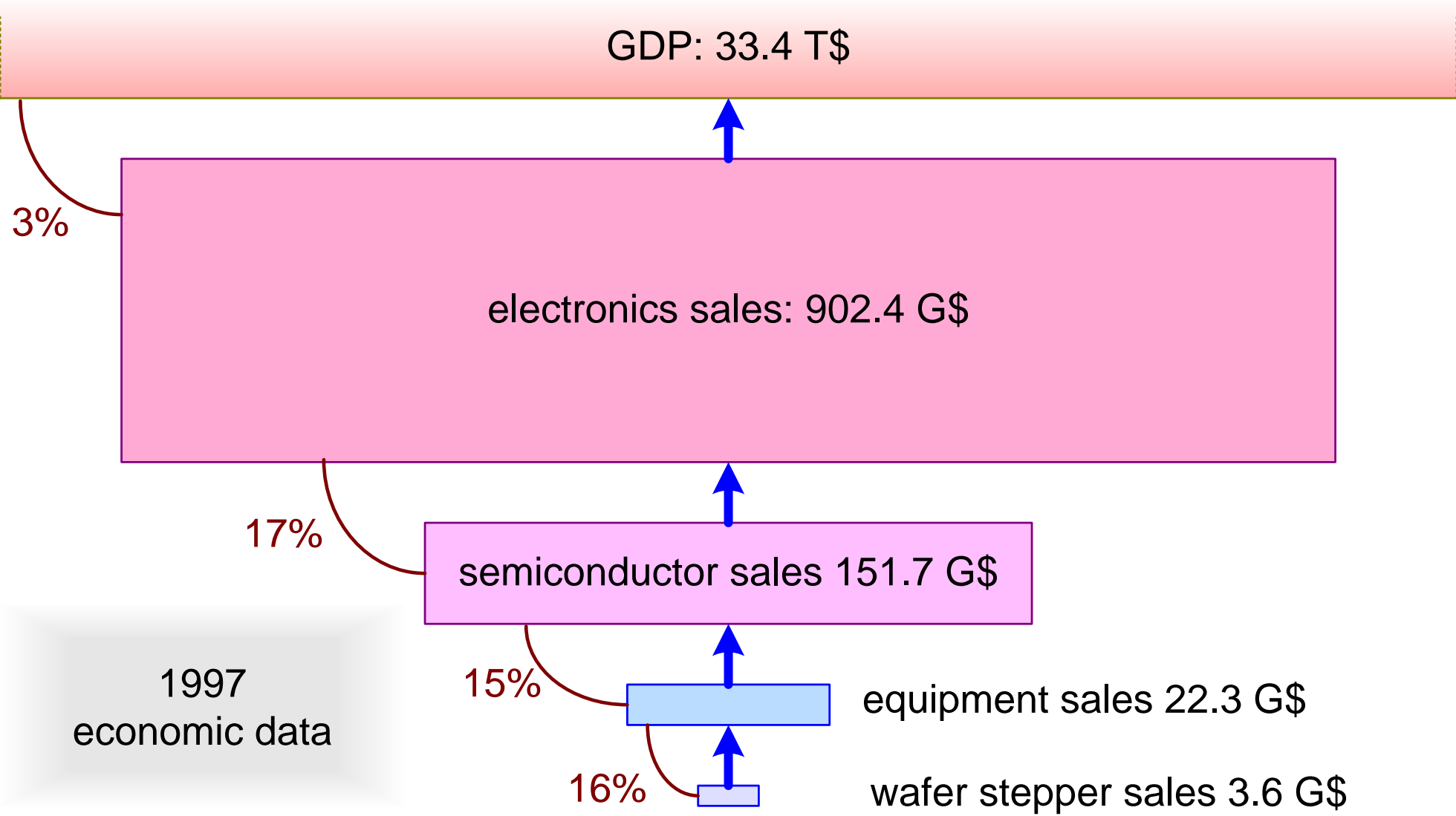
test rigs, prototypes, virtual models, and simulations

*save* a lot of money

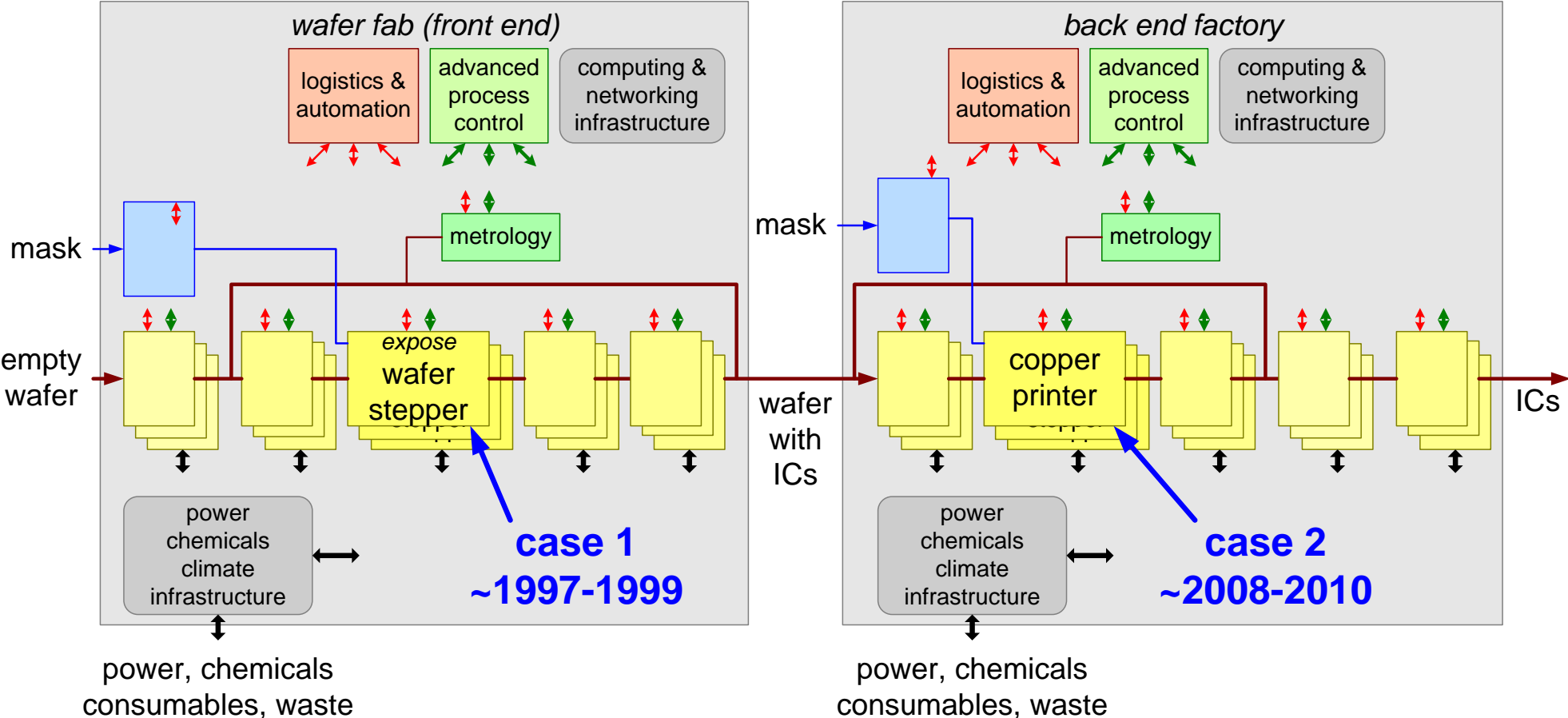
# Figure Of Contents™



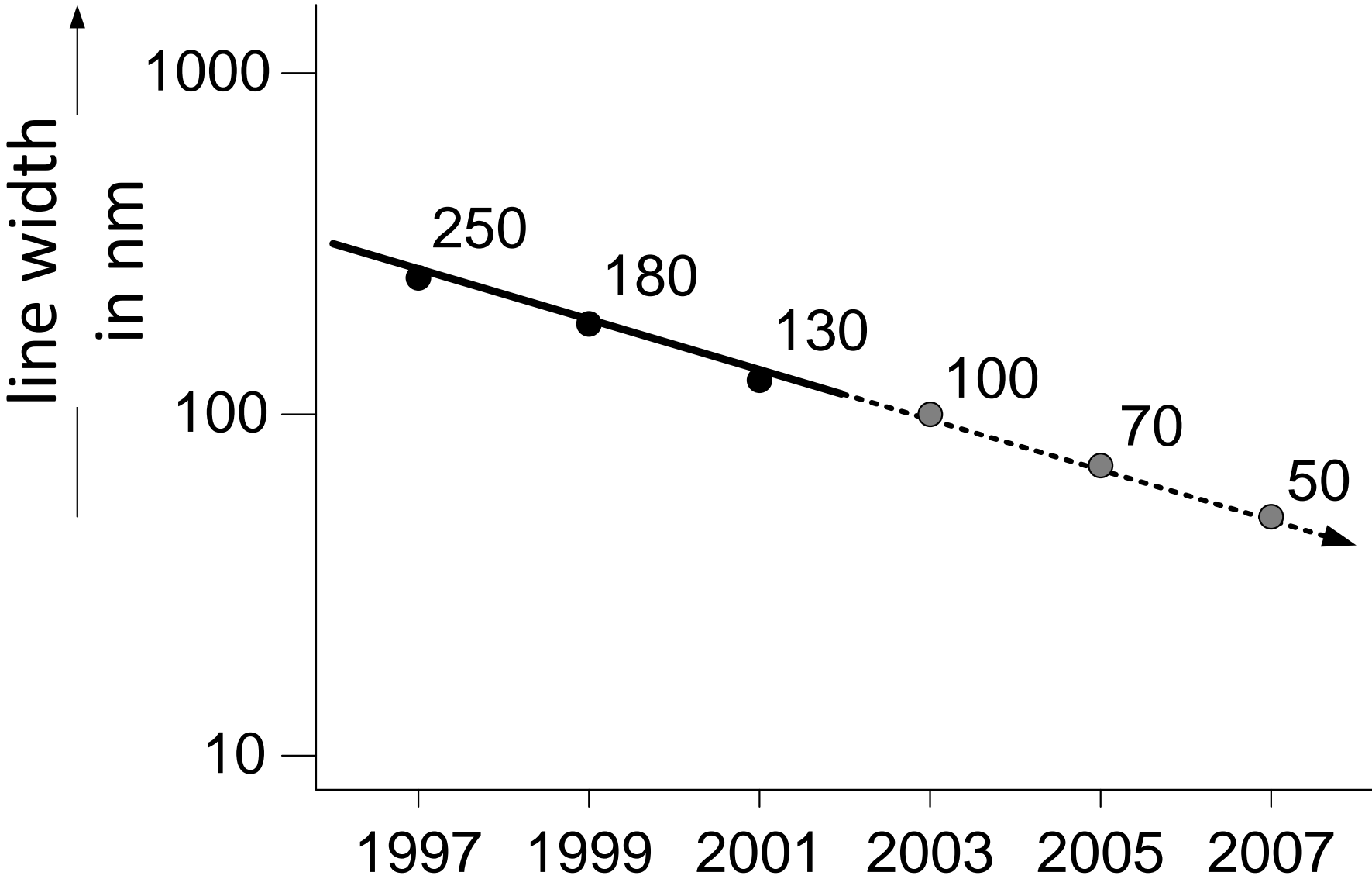
# Semiconductor Economics

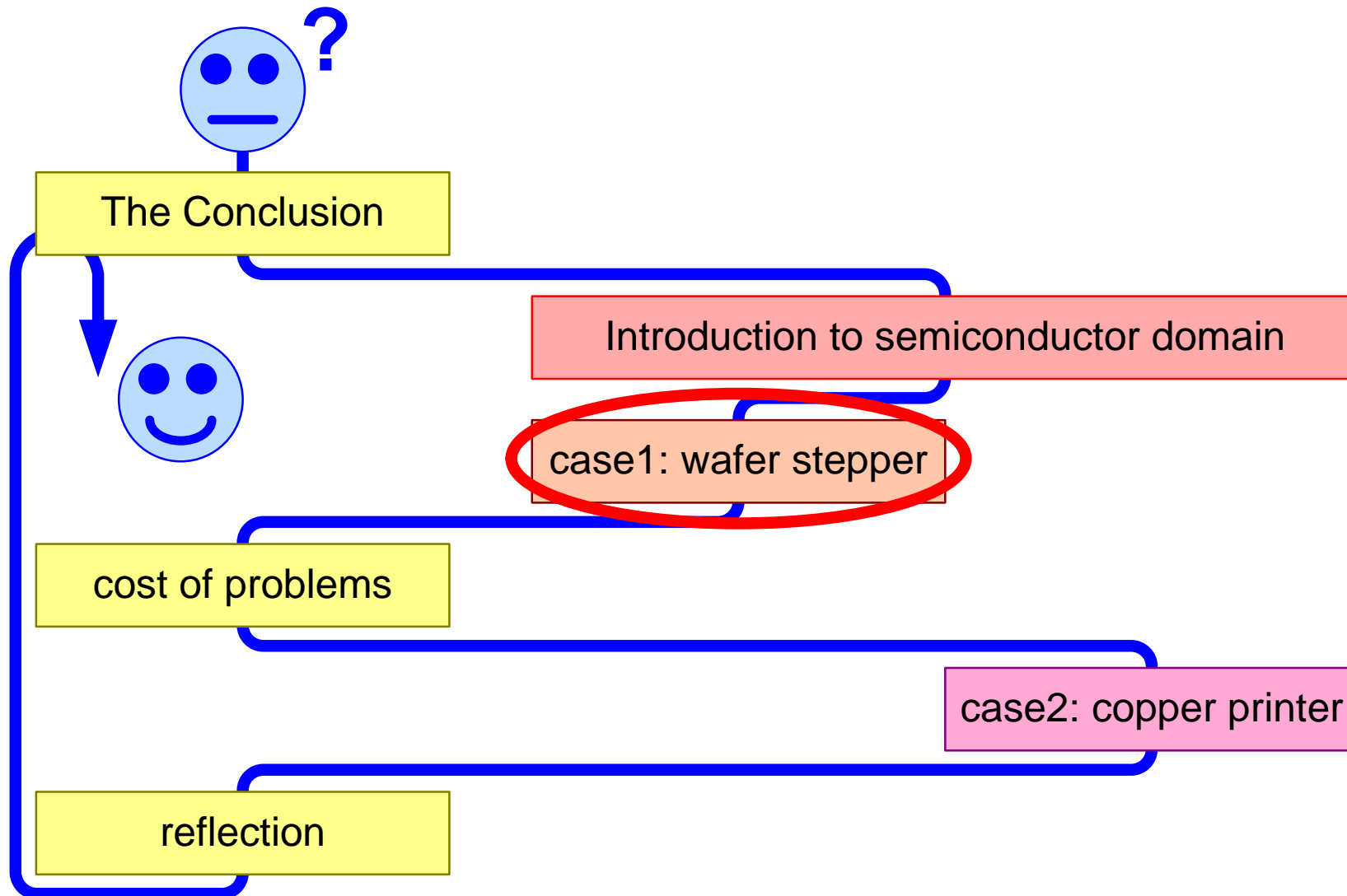


# Semiconductor IC manufacturing



# Moore's law



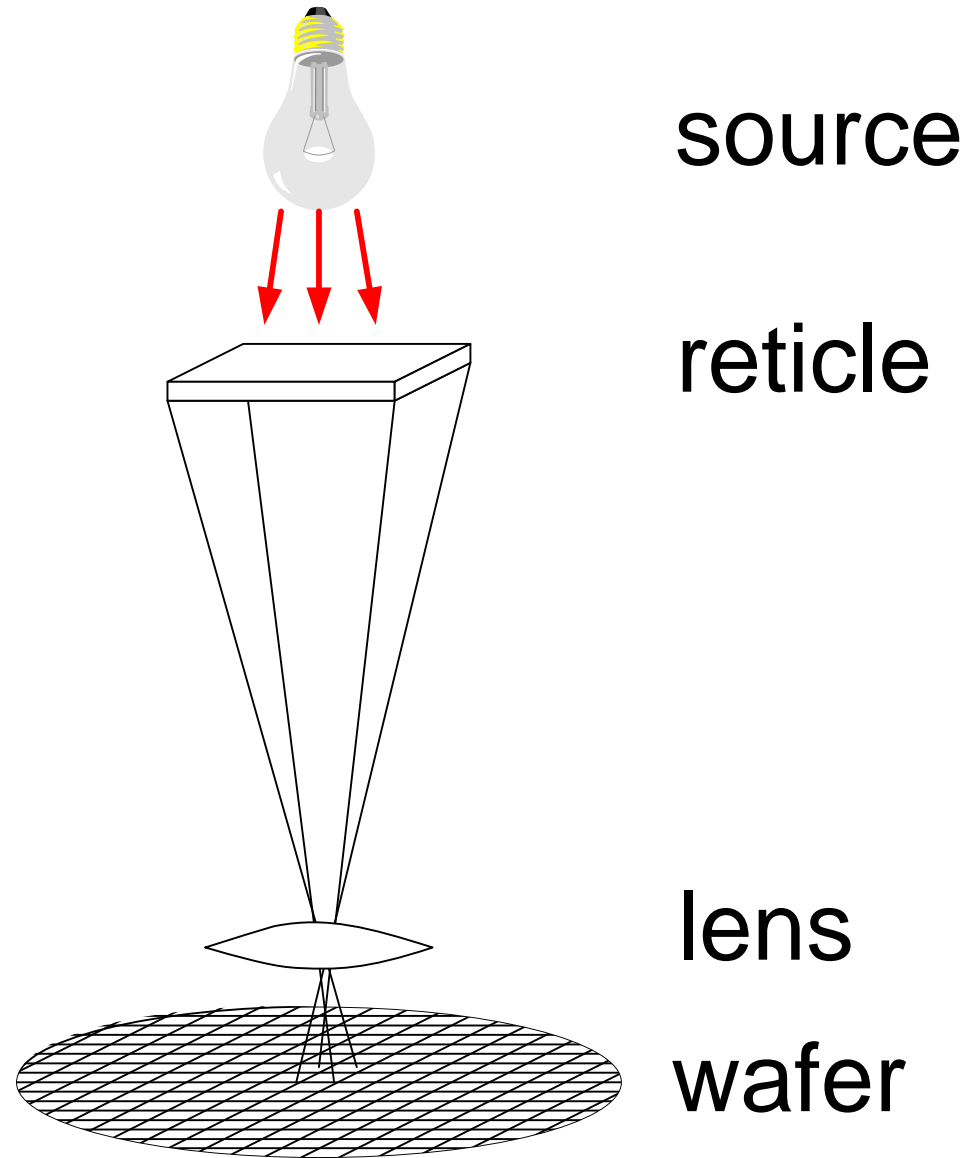


# Twinscan AT1100

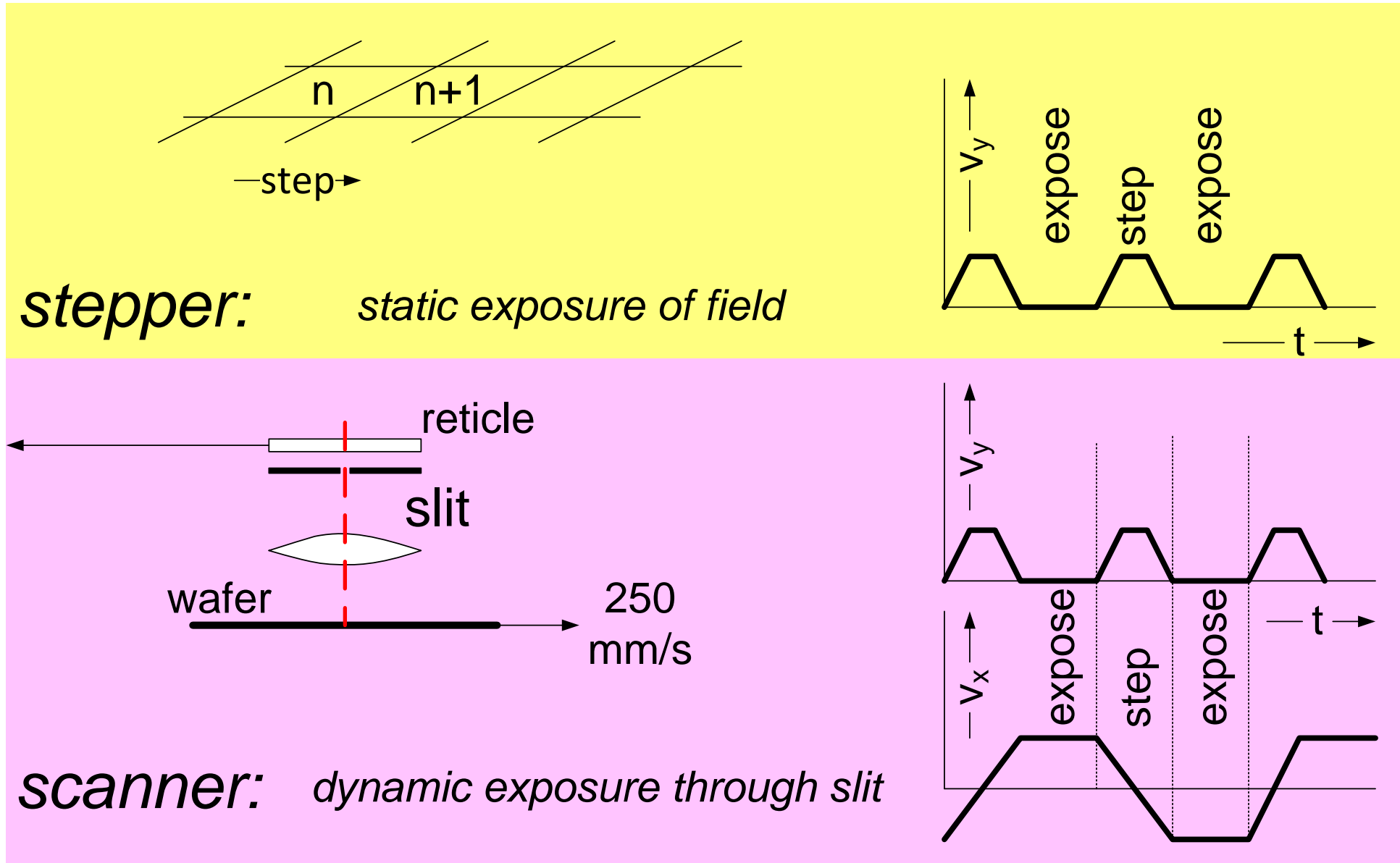


# What is a waferstepper

---

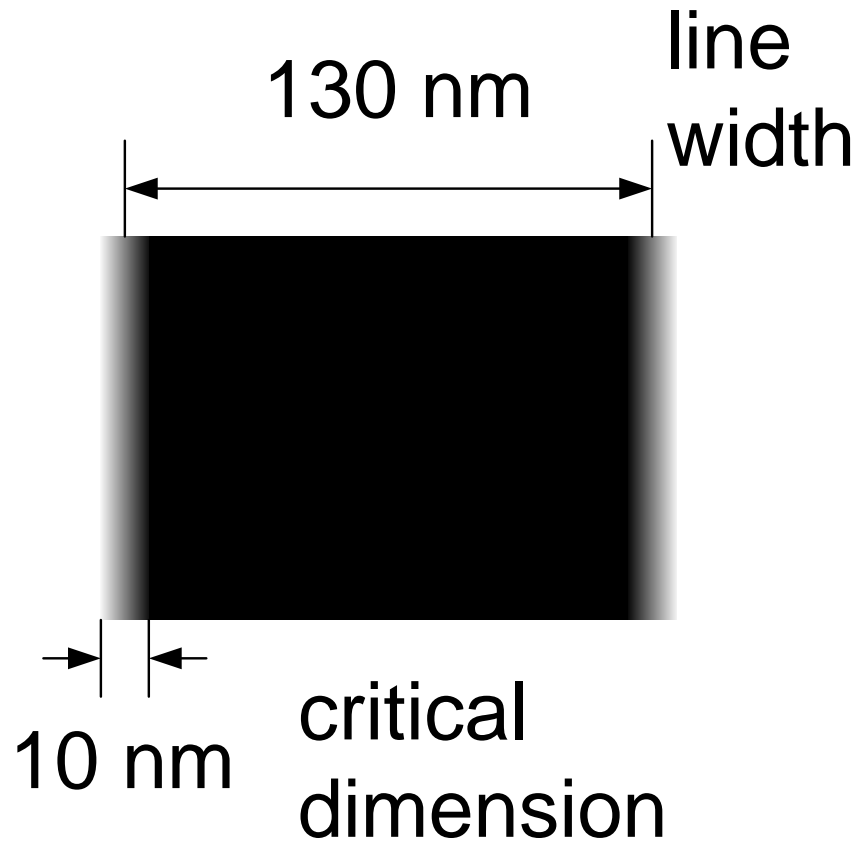


# From stepping to scanning

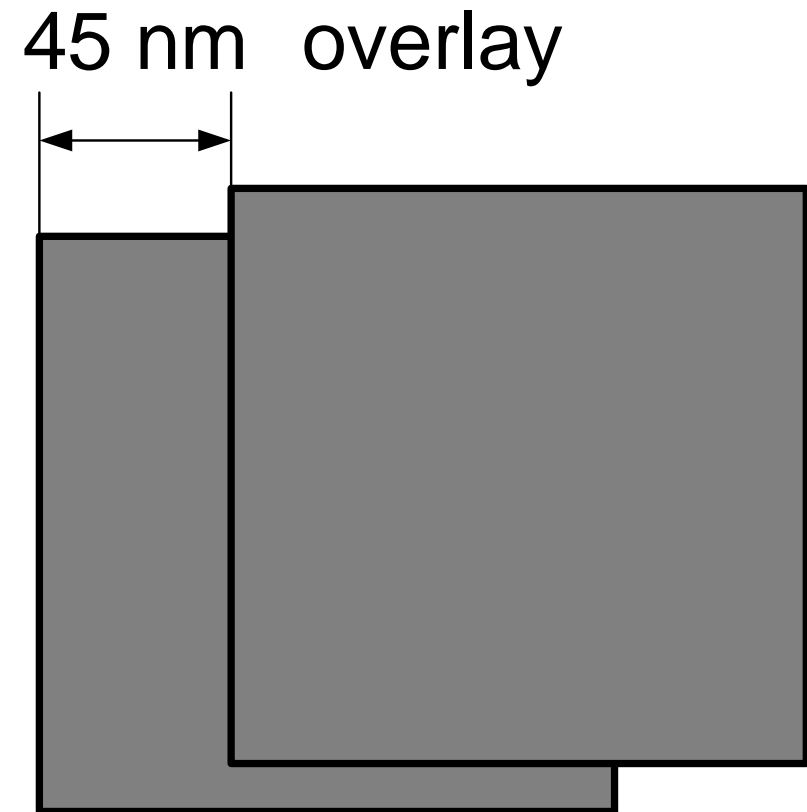


# Key specifications waferstepper

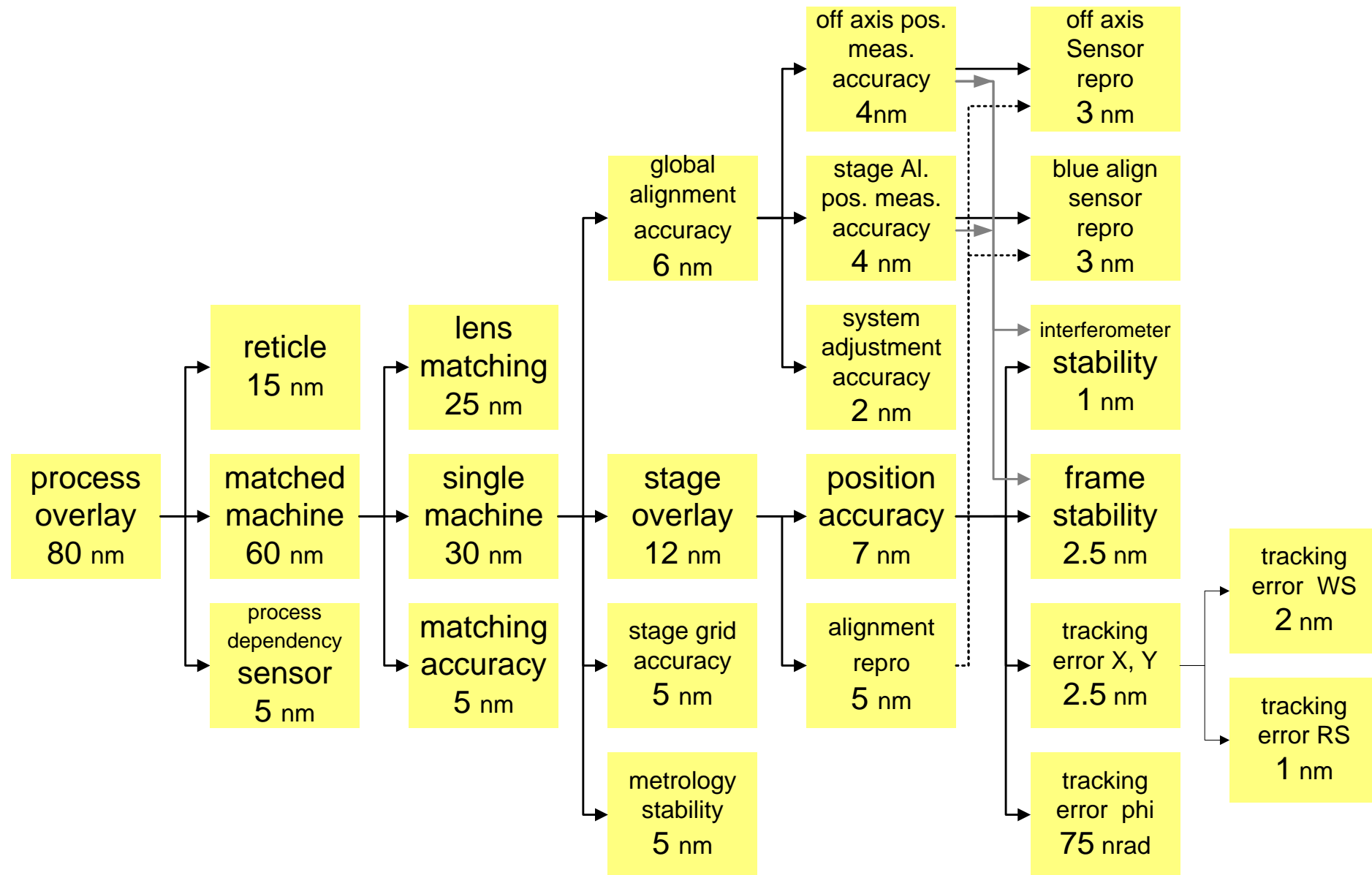
## imaging



## alignment




# Overlay budget (1999)

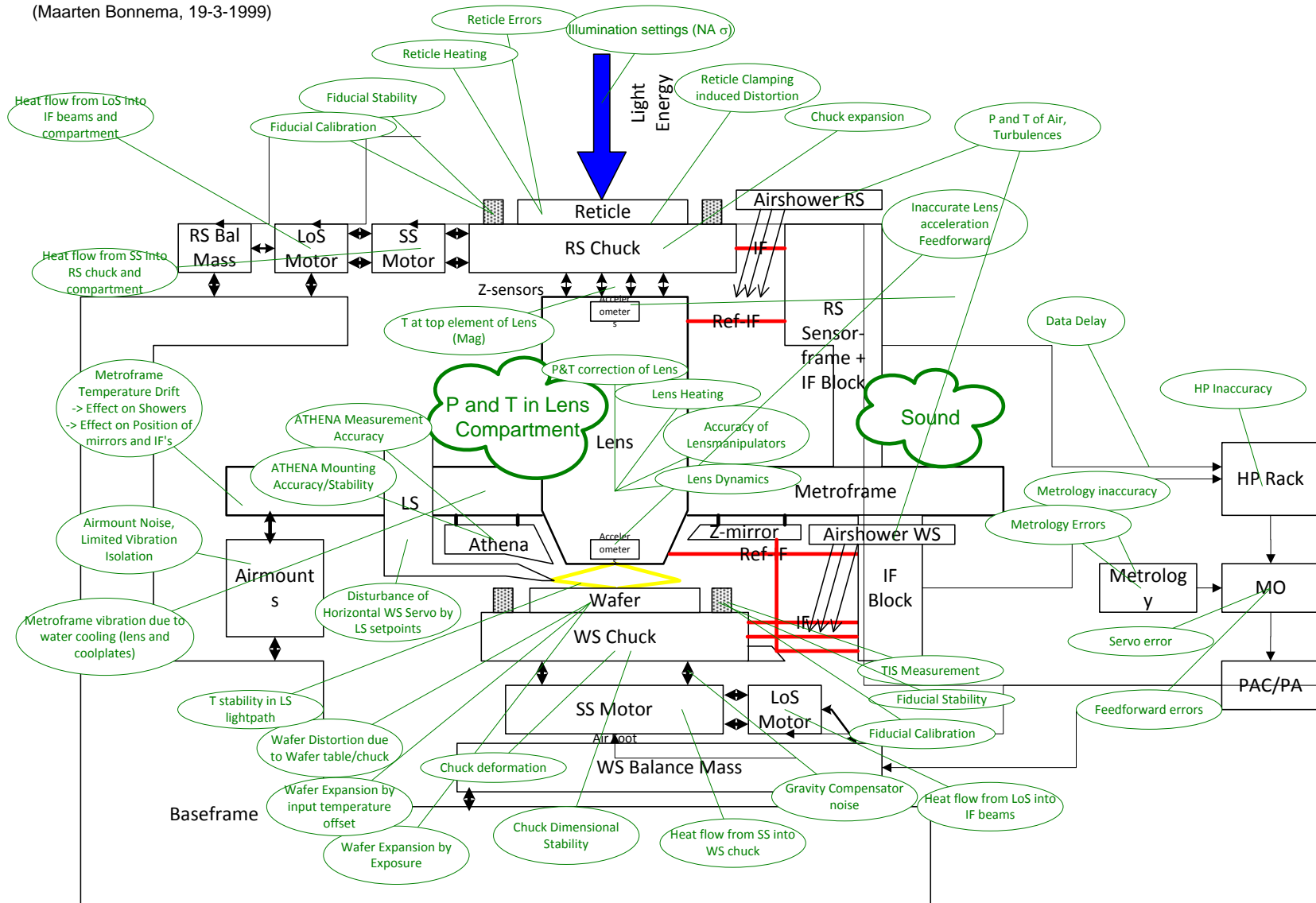


# Everything influences overlay

## Overlay Influence Diagram.

(Maarten Bonnema, 19-3-1999)

 : Fiducial



# Integration of Overlay

---

test models for  
critical functions

*scanning stage*

build core  
machine

*stages, lens,  
alignment, level  
sensor,  
illumination*

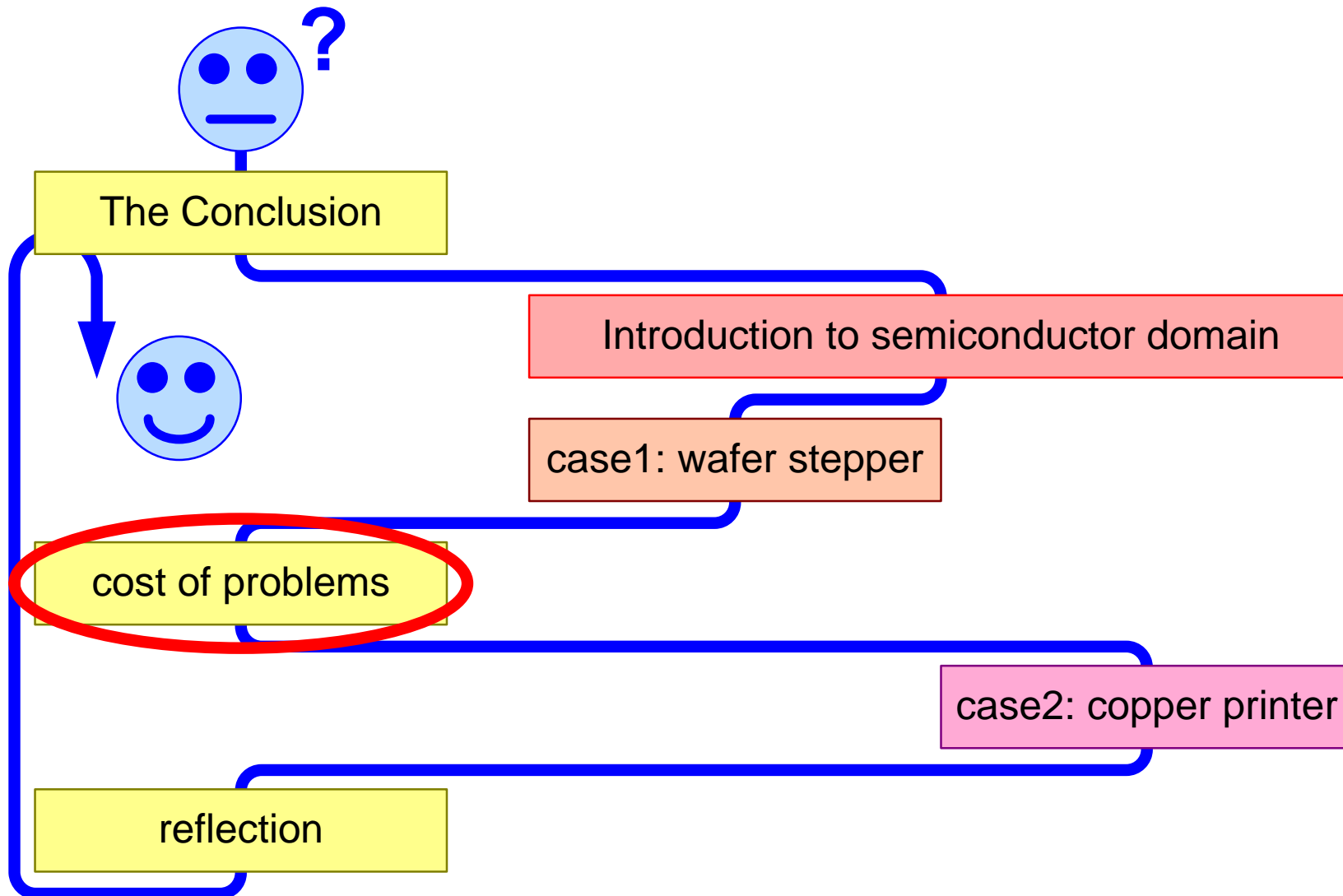
run manual  
sequence

*load wafer,  
align, focus,  
dose setting,  
and many more*

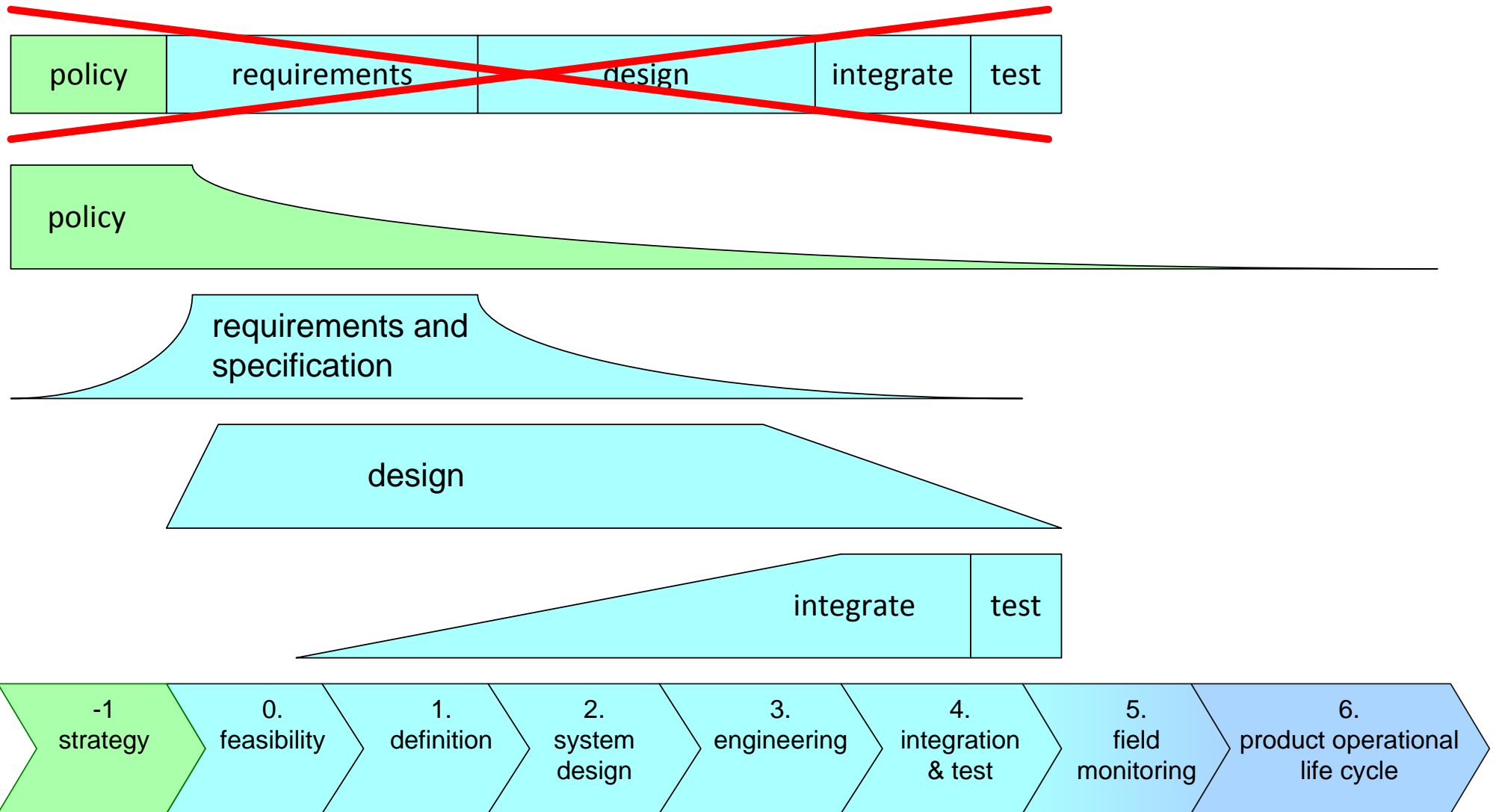
expose

*process wafer  
measure overlay*

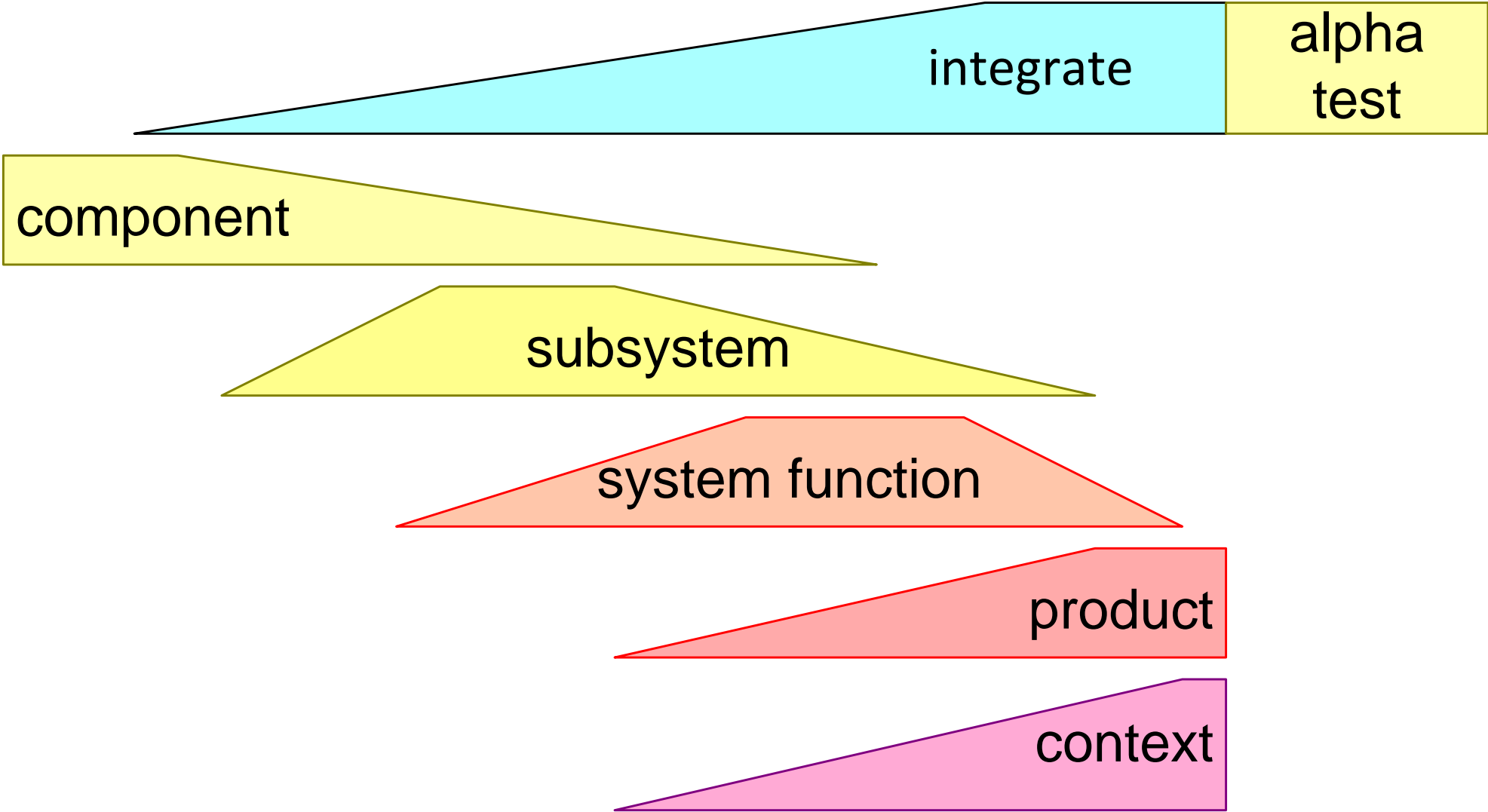
blood, sweat, and tears  
trouble shooting  
and learning



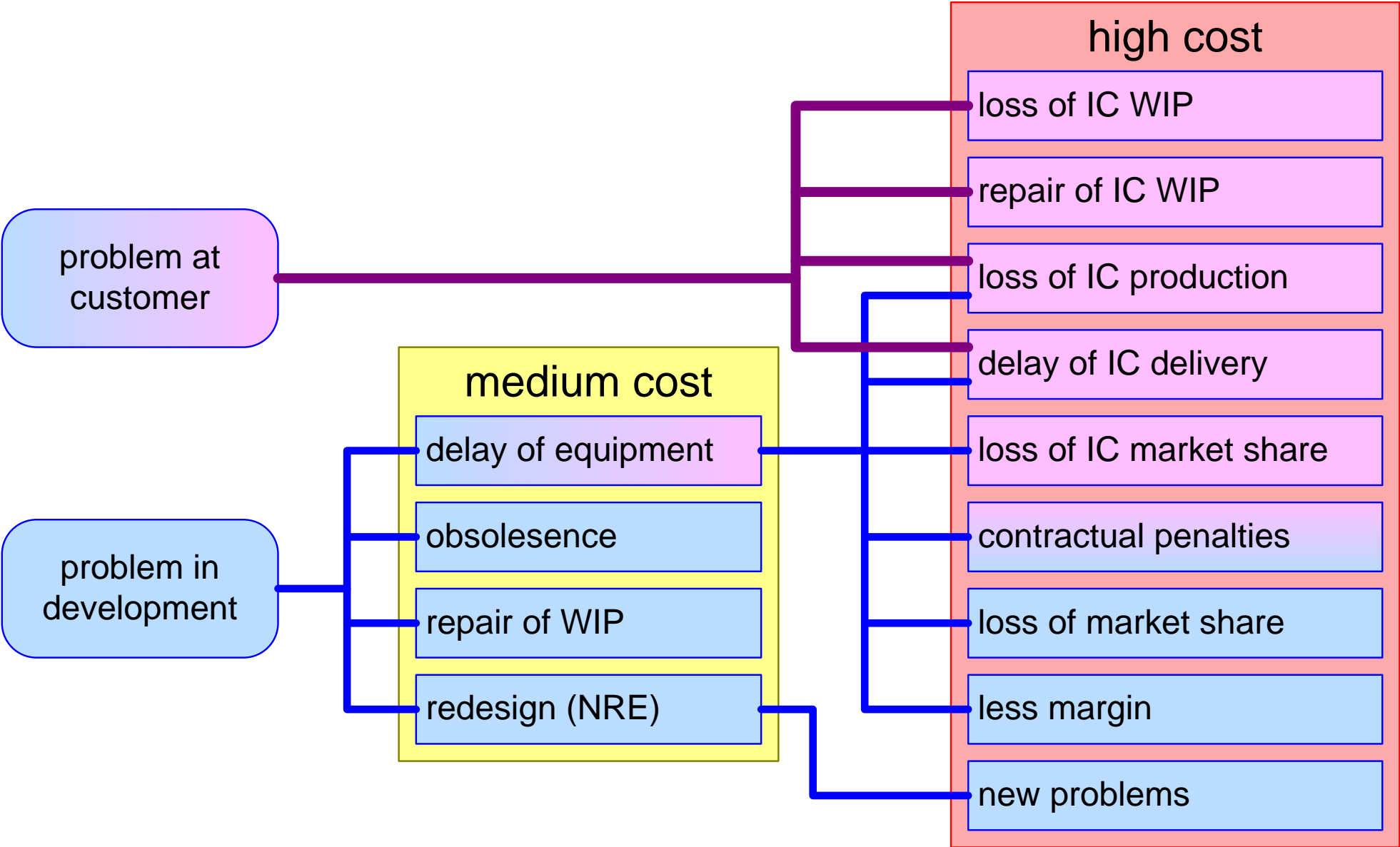
# Typical Concurrent Product Creation Process



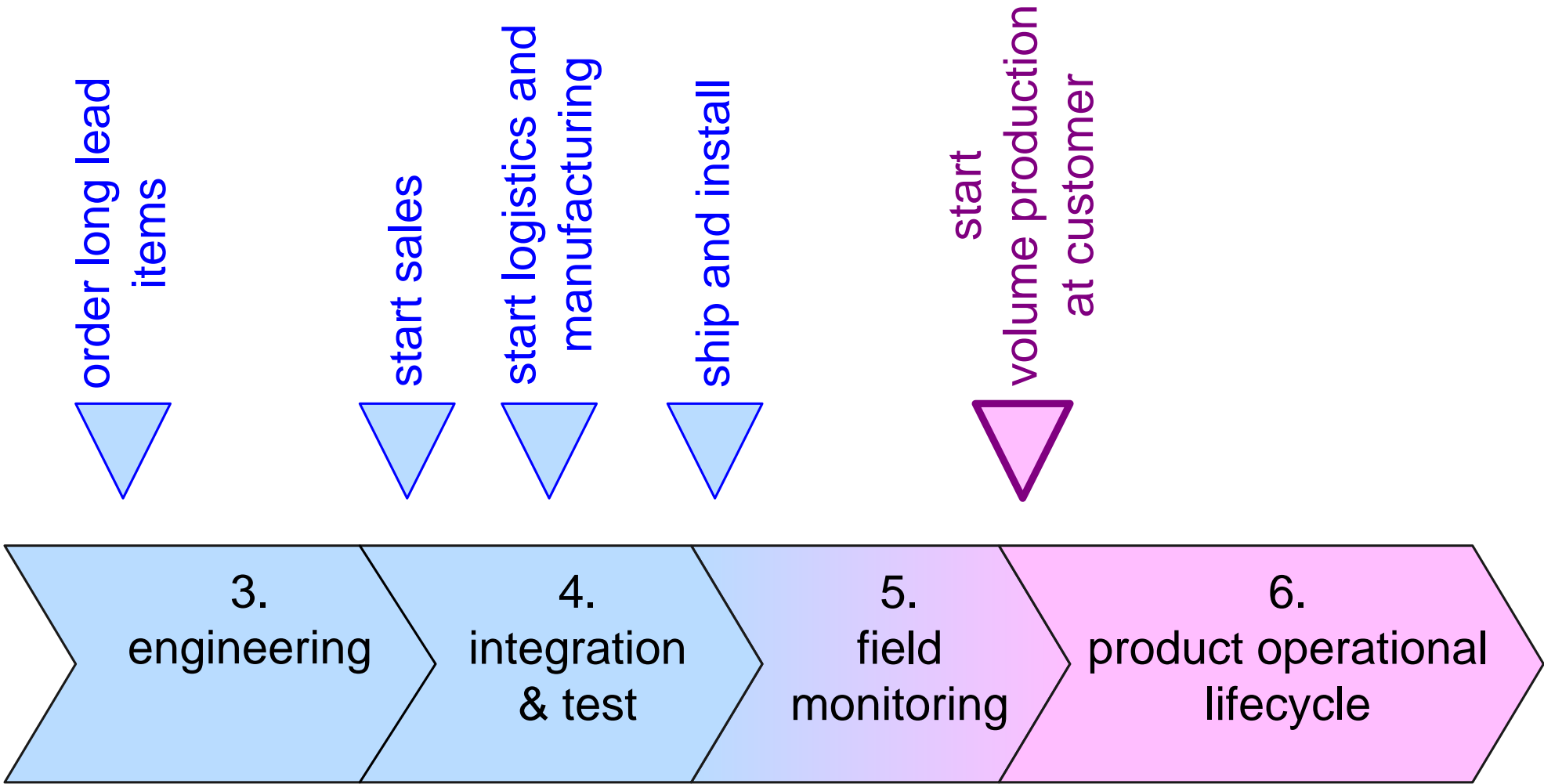
# Integration Takes Place in a Bottom-up Fashion

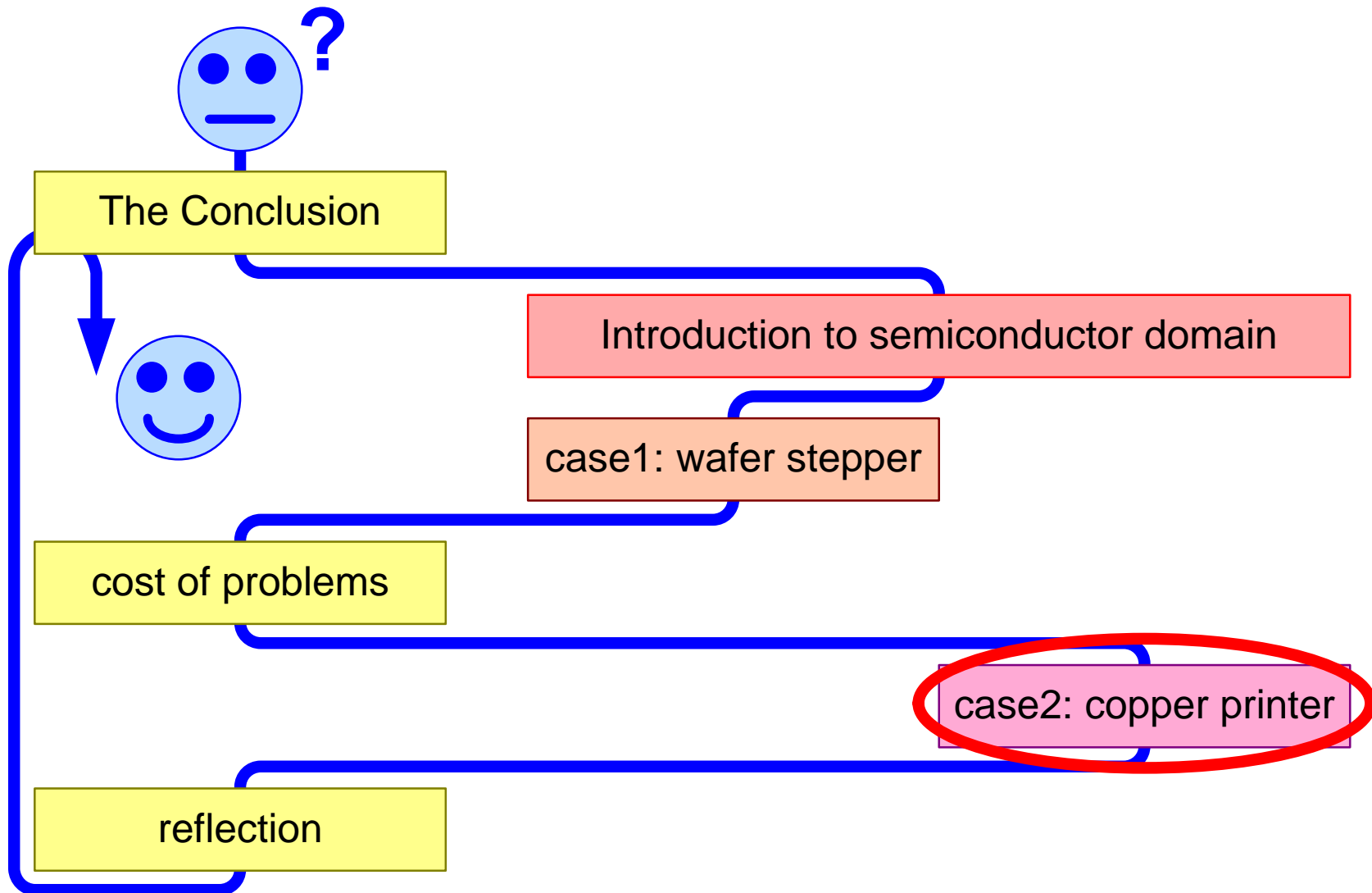


# Costs of Encountered Problems

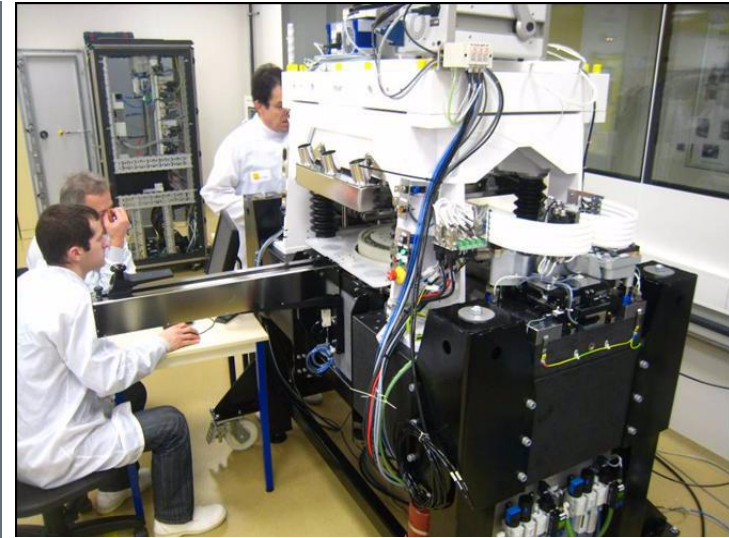
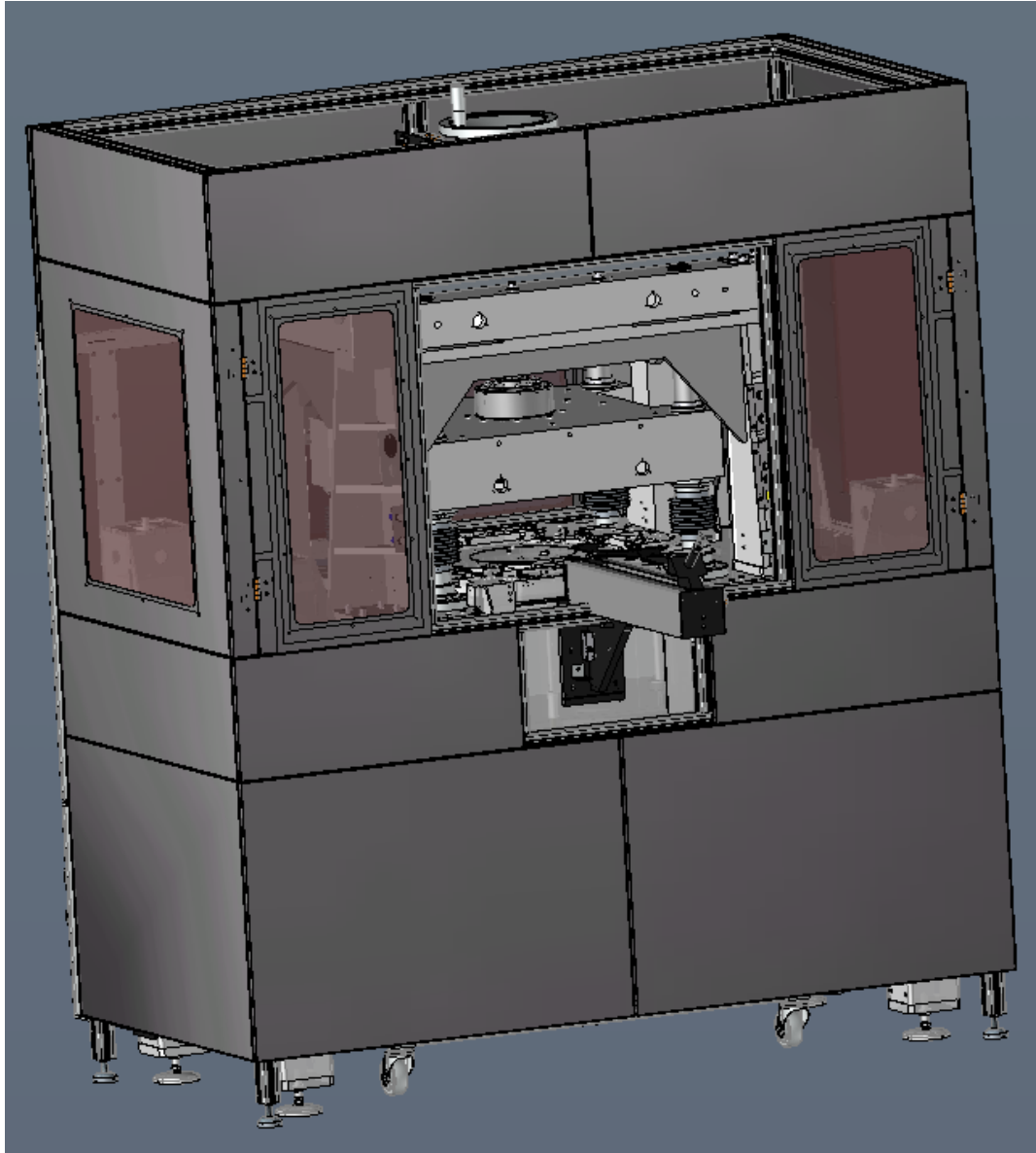


# Cost Related Milestones

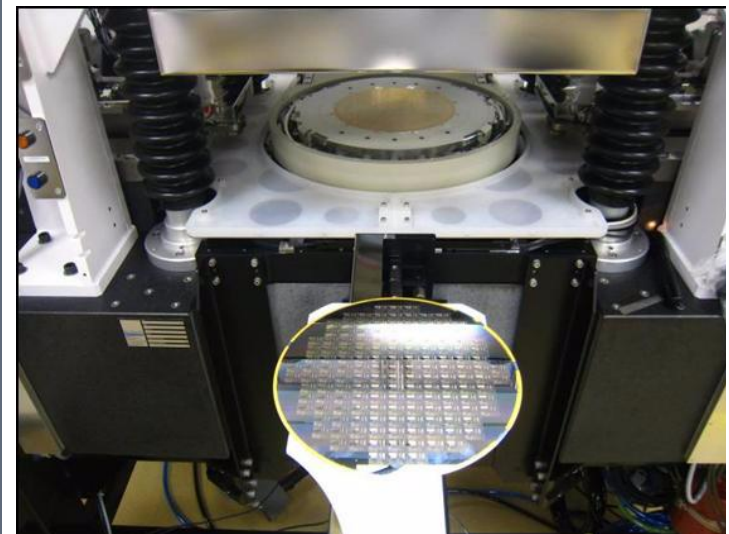




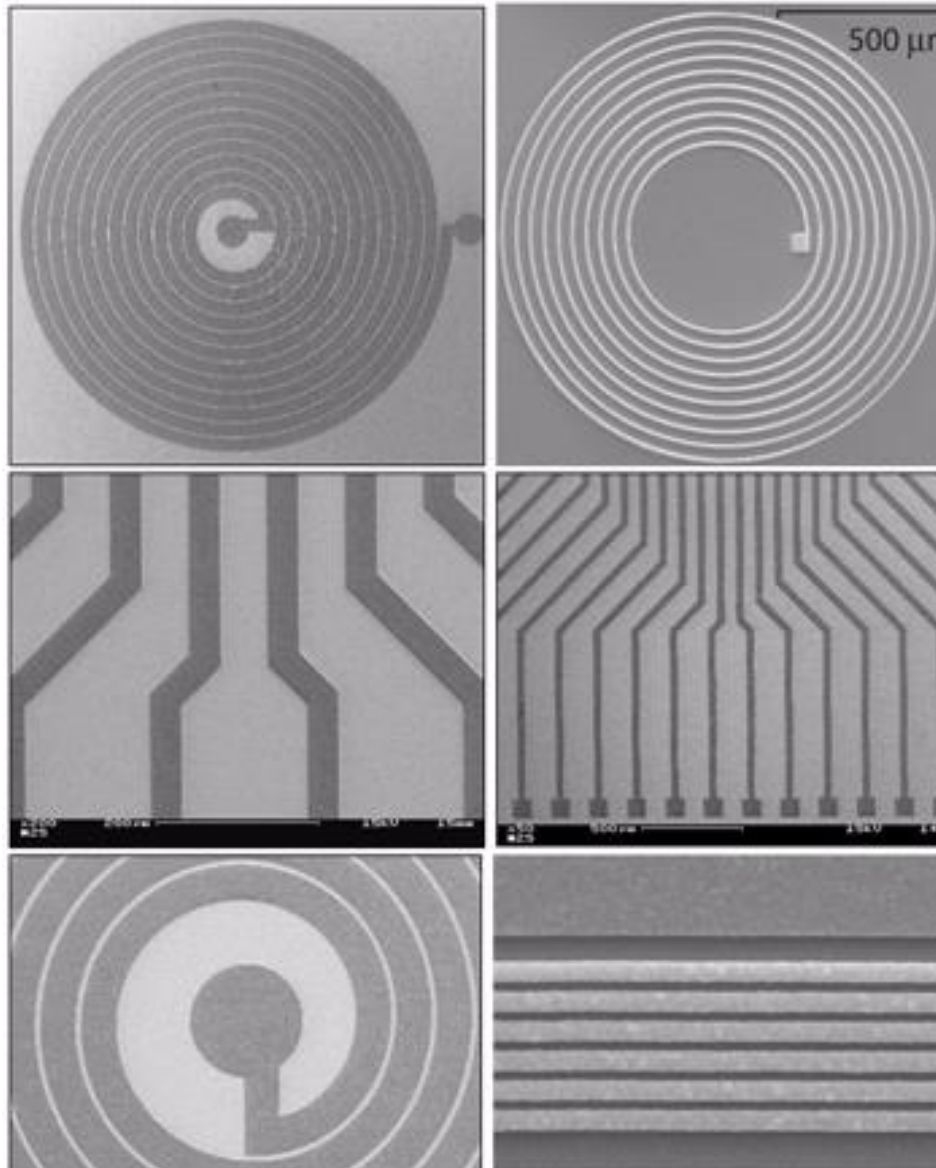
# Case 2 Replisaurus Copper Printer



courtesy Replisaurus  
[www.replisaurus.com](http://www.replisaurus.com)



# Example of printed copper structures

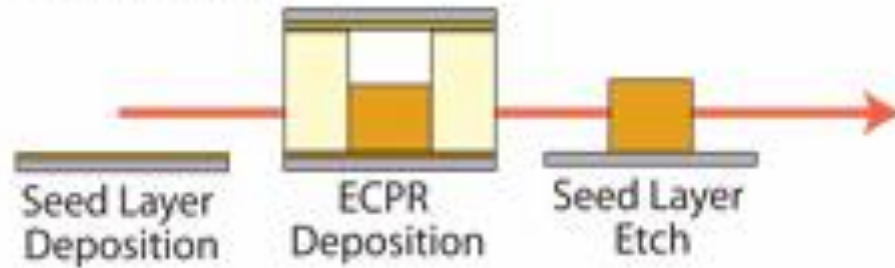


courtesy Replisaurus  
[www.replisaurus.com](http://www.replisaurus.com)

# ECPR technology replaces 6 process steps by 1 step

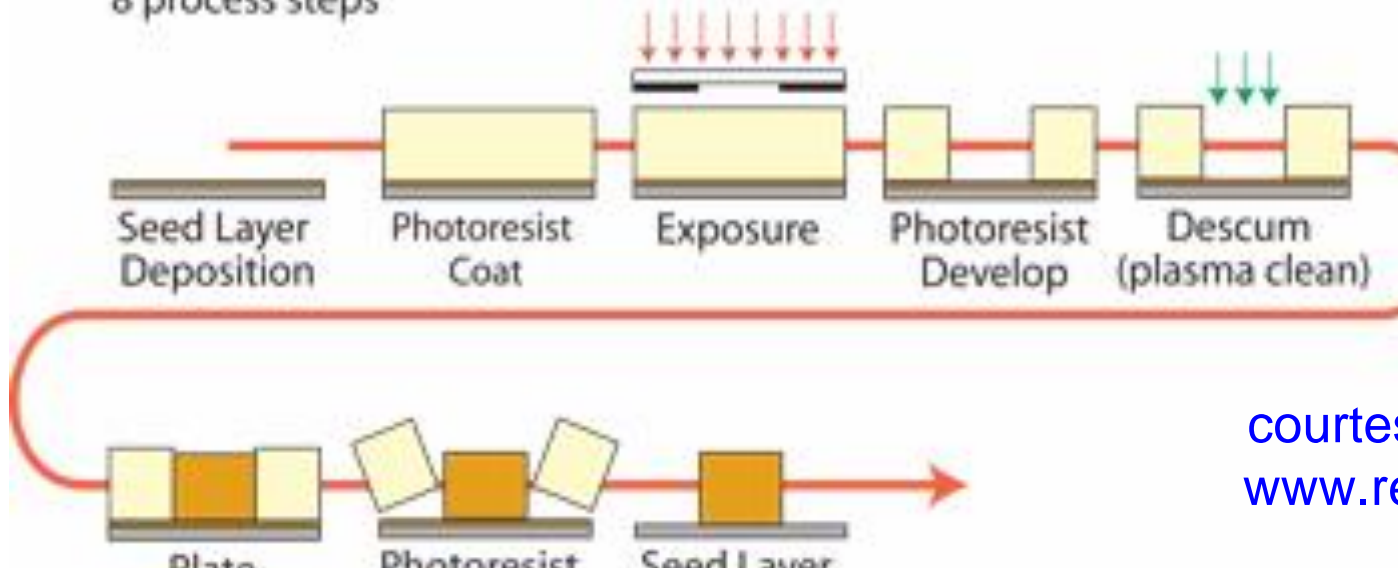
## ECPR - ElectroChemical Pattern Replication

3 process steps



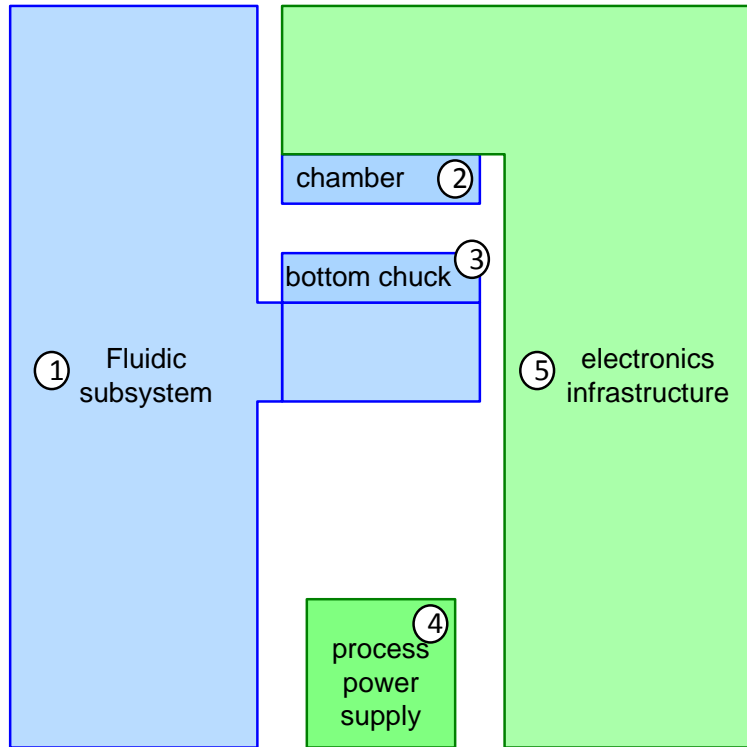
## Conventional lithography based metallization

8 process steps

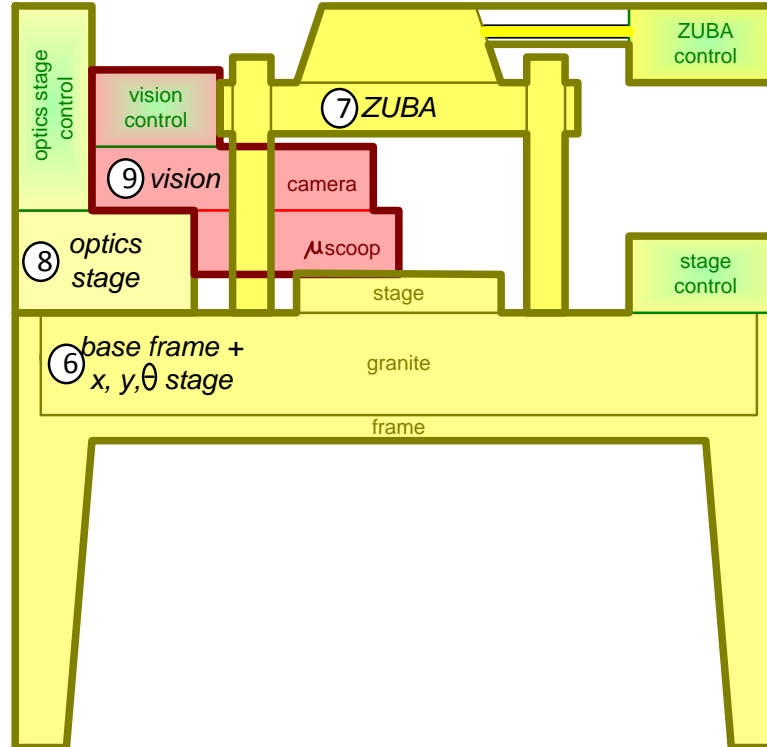


courtesy Replisaurus  
[www.replisaurus.com](http://www.replisaurus.com)

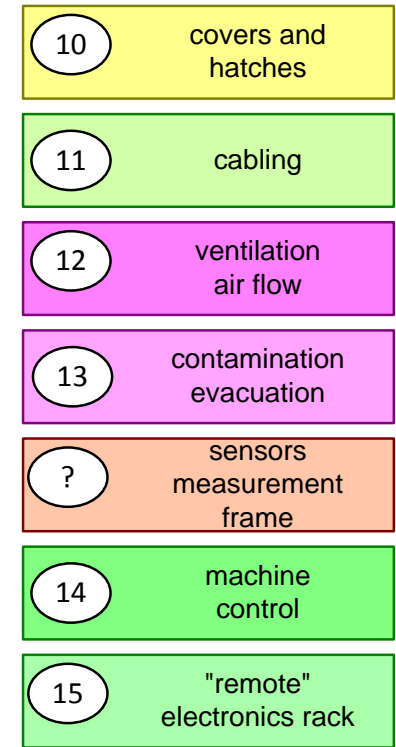
# Decomposition in sub systems



back side view

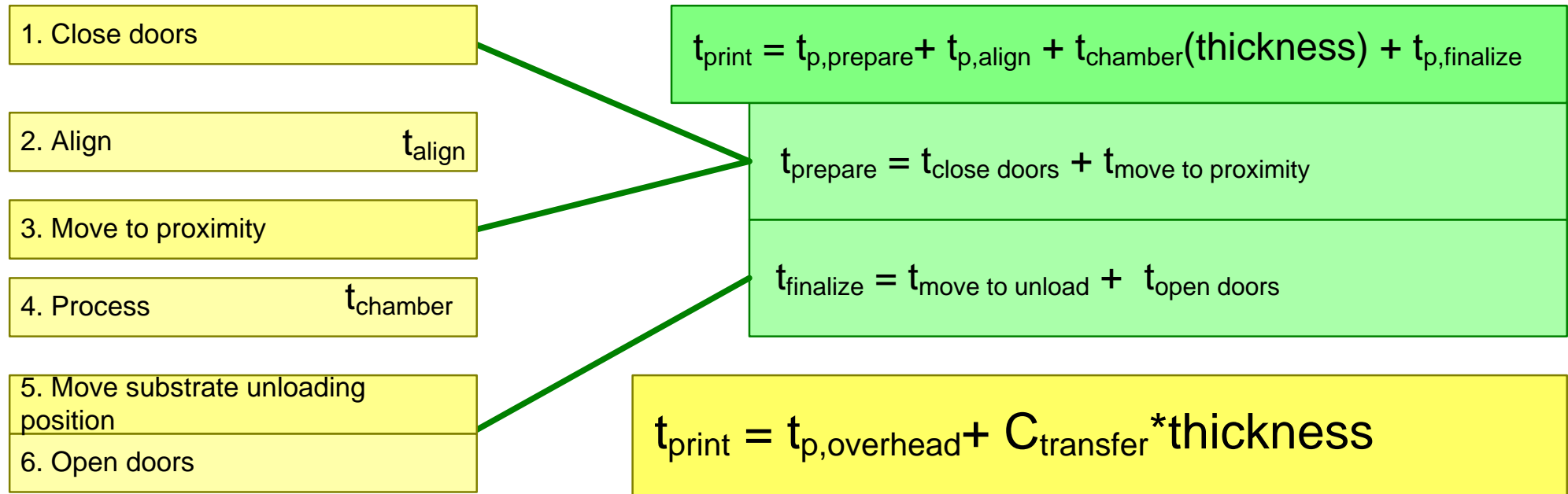


front side view



integrating

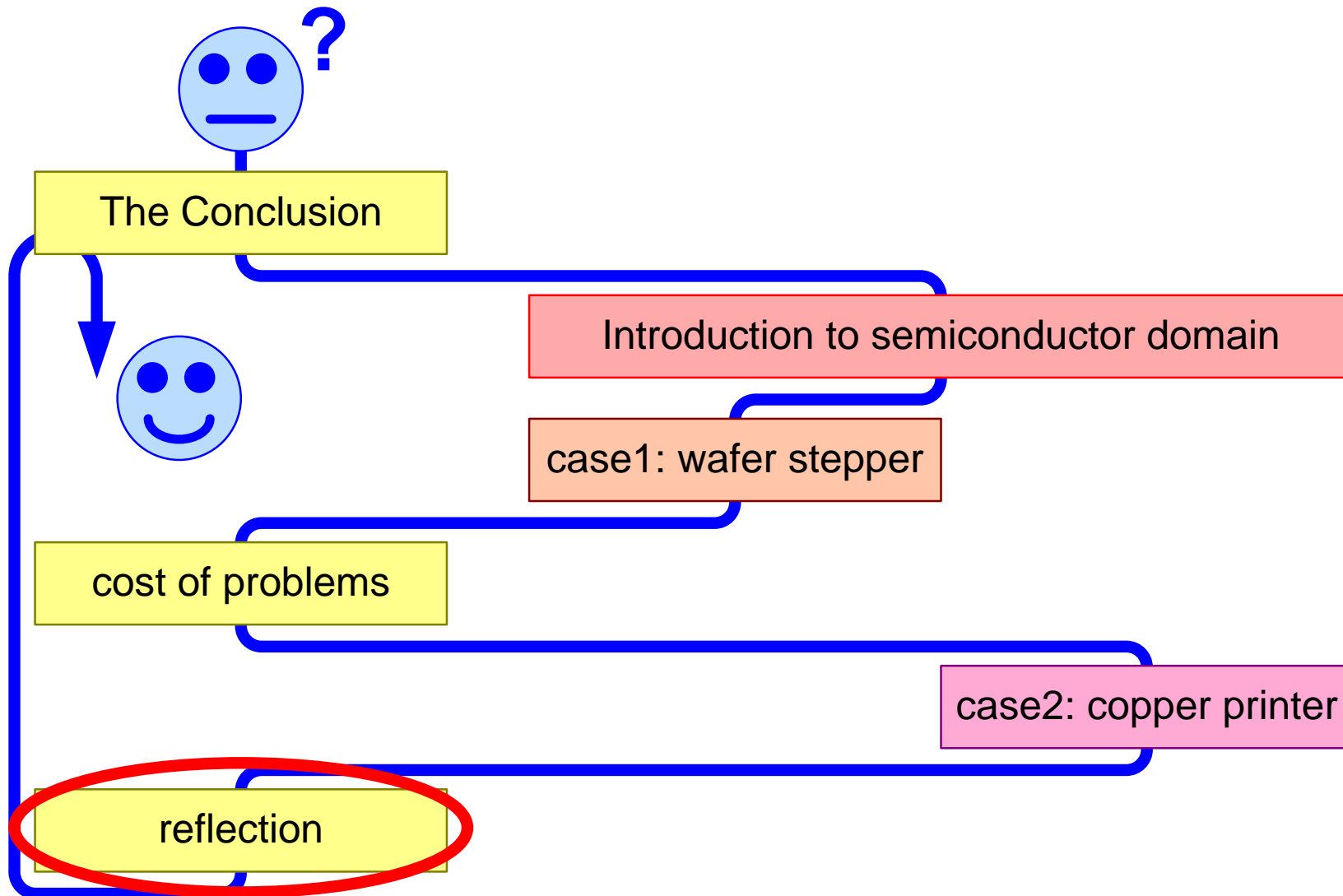
# Ca. 2 days per quarter used for simple models



*note: original diagram was annotated with actual performance figures for confidentiality reasons these numbers have been removed*

# Continuous Modeling and Learning

200mm ECPR tools	300mm ECPR tools. Can be configured with 200 or 300mm kits.				Case: Metal Printer
<p>2006 R&amp;D 1.0</p>	<p>2007 REX 1.0</p>	<p>2008 R&amp;D 2.0</p>	<p>2009 REX 2.0</p>	<p>2010 Alpha 1.0</p>	
<p>200mm hydraulic non-aligned tool for chamber &amp; process development</p>	<p>First aligned ECPR dev. tool. 200/300mm compatible.</p>	<p>Integrated ECPR control. Non-aligned, Footprint, confinement</p>	<p>Production oriented print module. Cycle time, overlay, confinement &amp; footprint focus.</p>	<p>First integrated tool prefill – clean- print – seed etch.</p>	<p>courtesy Replisaurus</p>



# What We Teach:

---

functional decomposition

physical decomposition

modularity

interface management

seperation of concerns

low coupling between components/functions

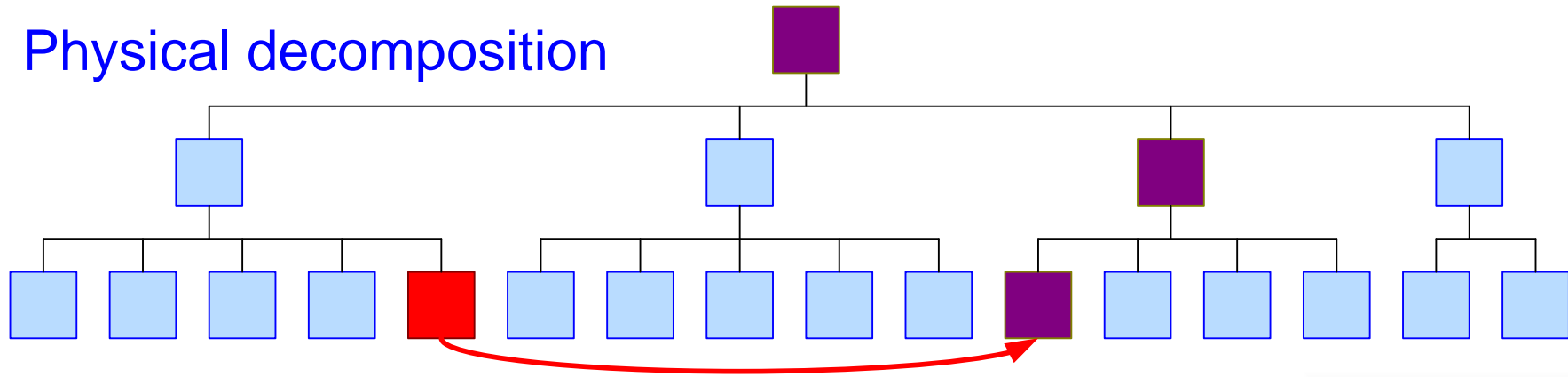
high cohesion within components/functions

SMART (Specific, Measurable, ...)

traceability

# Root Cause is Often Elsewhere

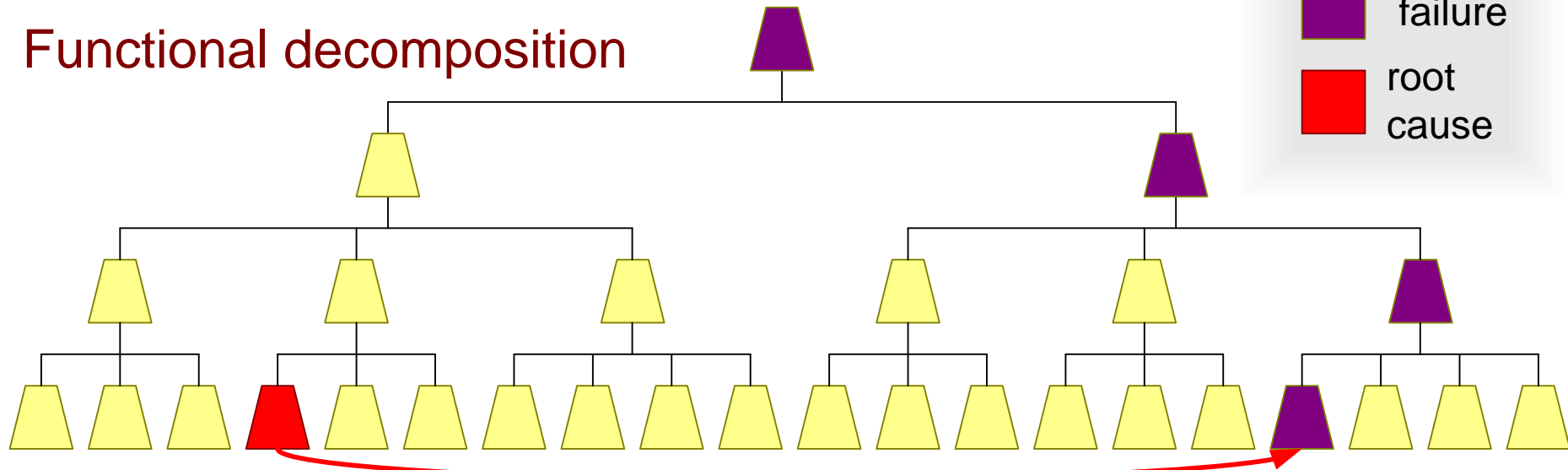
## Physical decomposition



legend

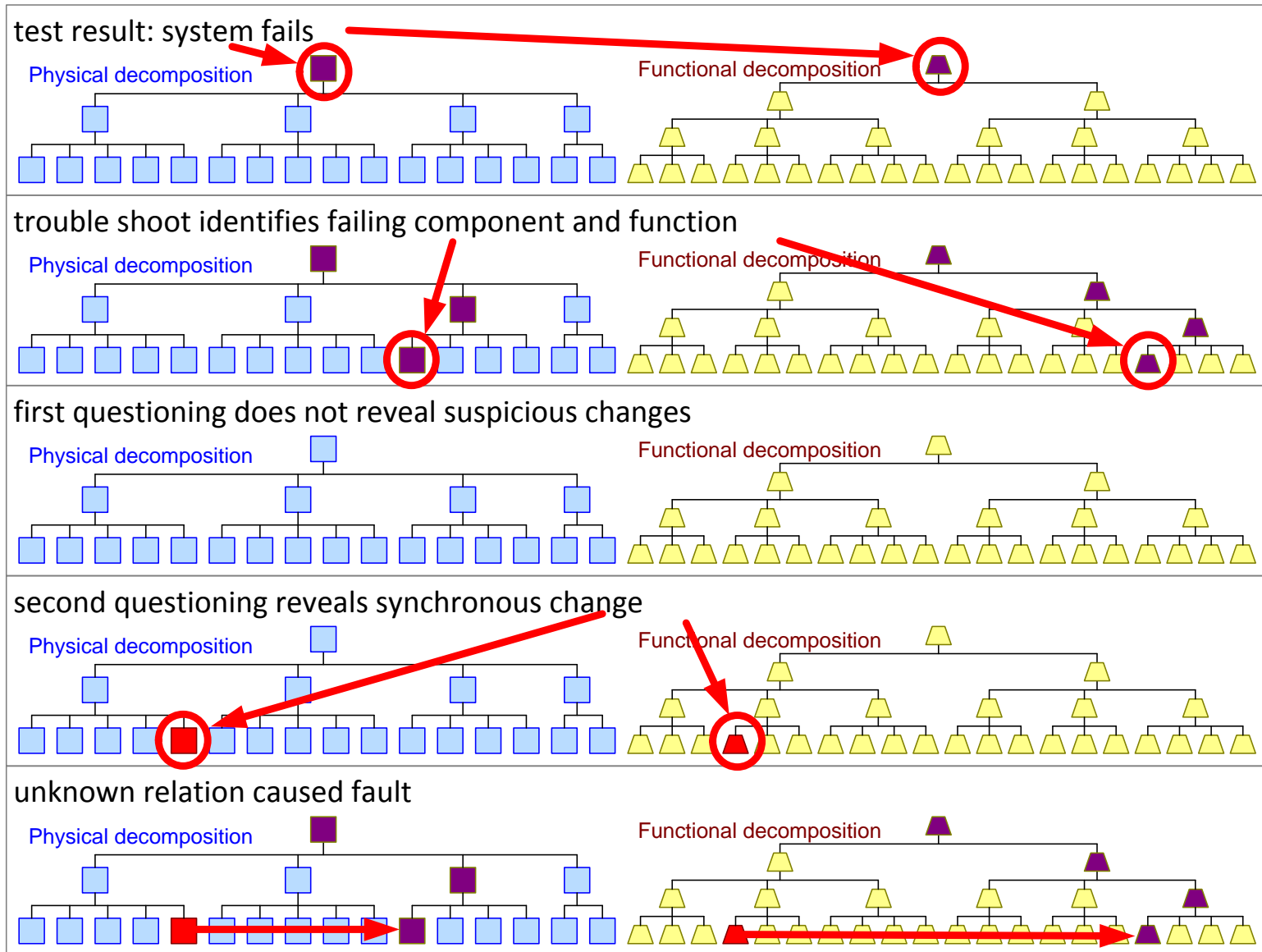
- failure
- root cause

## Functional decomposition

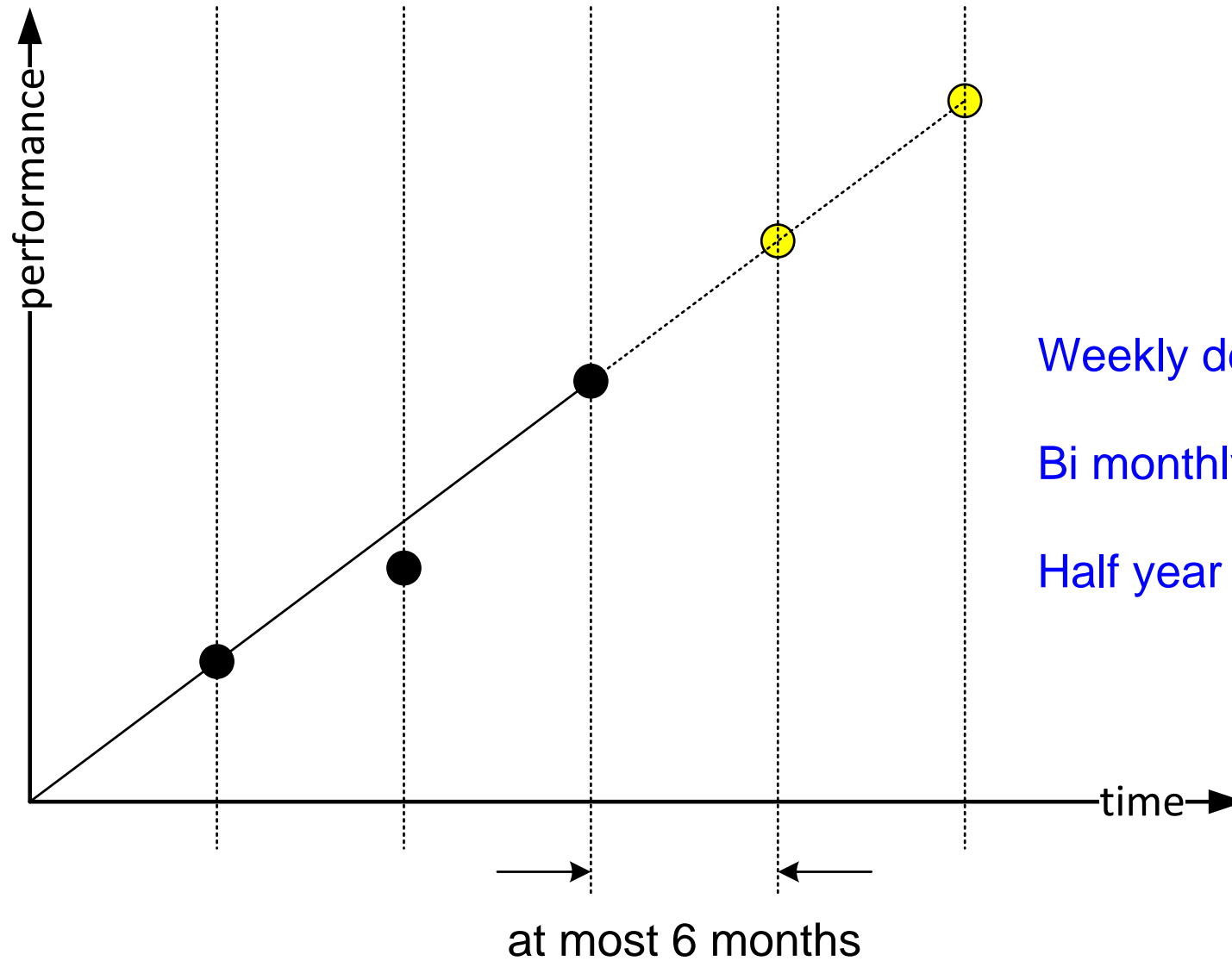


unknown or unexpected relation

# “Nothing has been changed...”



# Monitoring Performance Targets

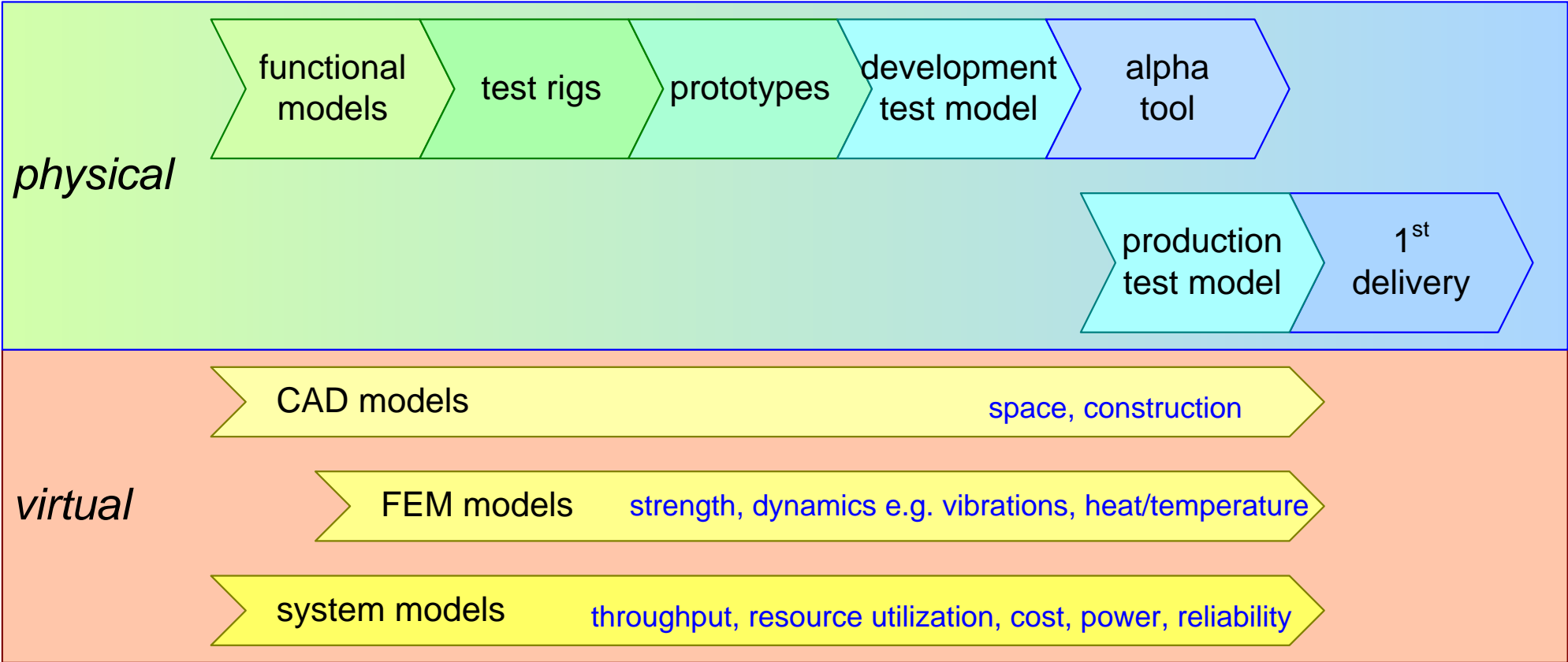


Weekly design meetings

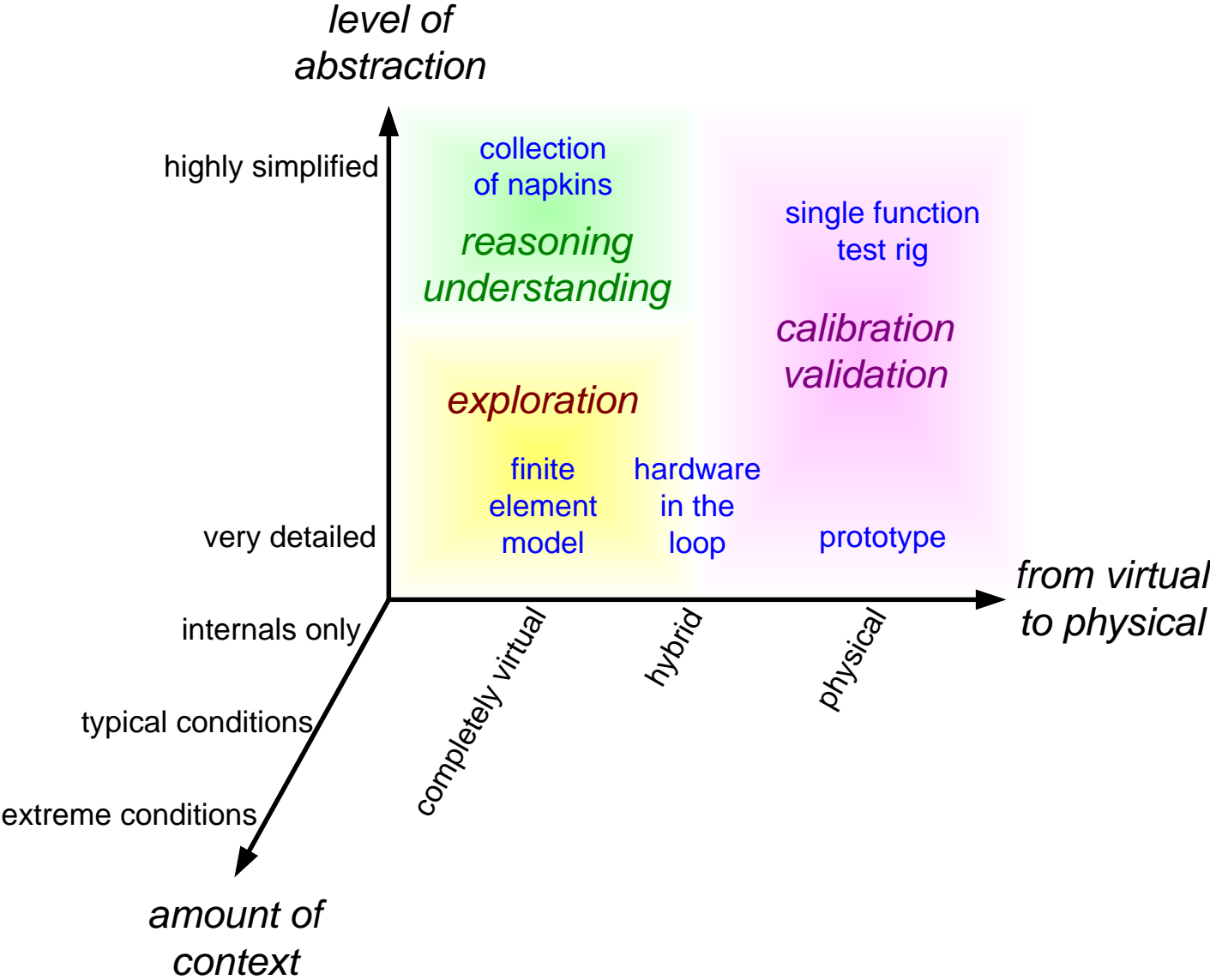
Bi monthly design reviews

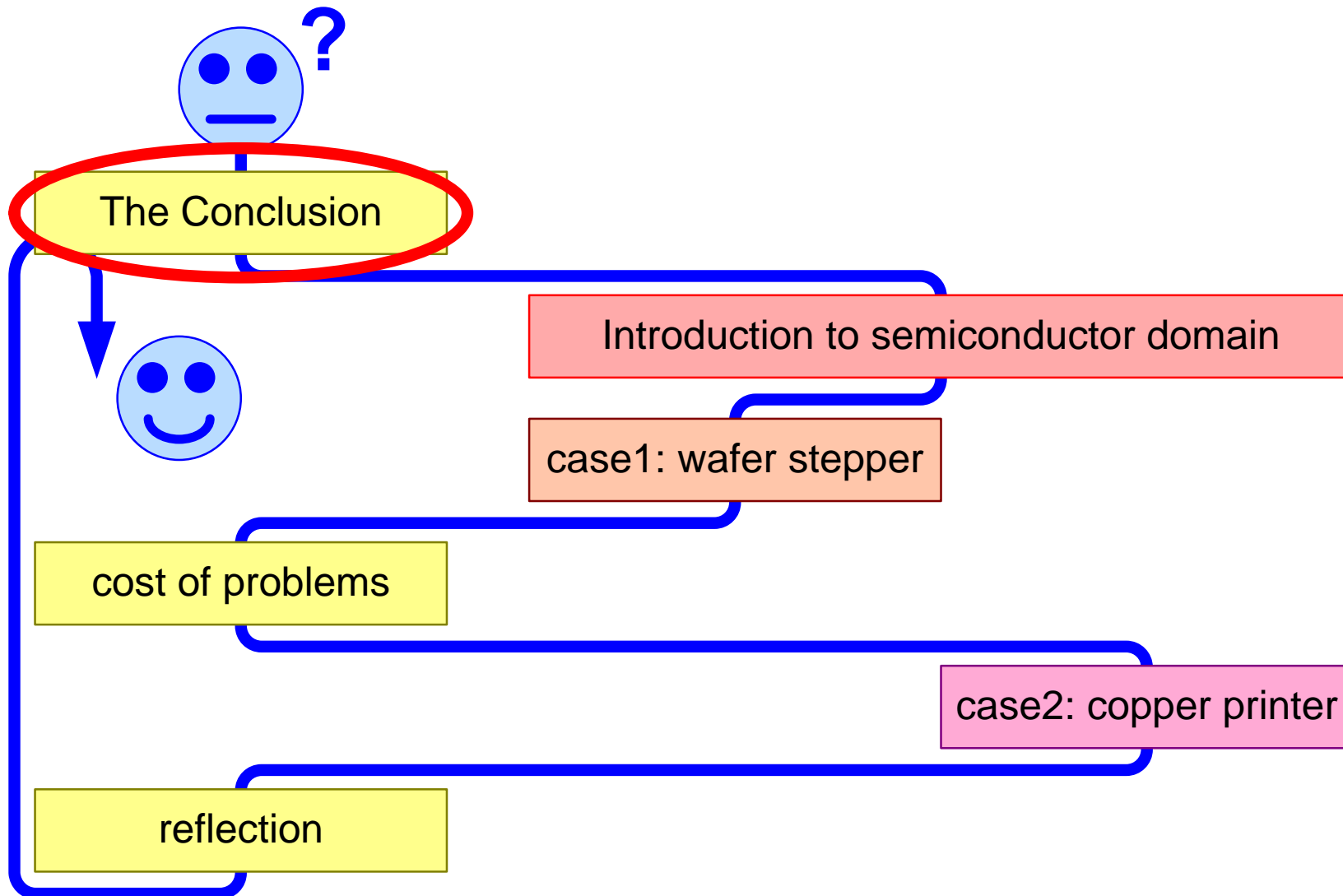
Half year milestones

# Phasing of Models



# Modeling Space





# Conclusion from Semiconductor Cases

## *semiconductor domain conclusions*

performance increase in semiconductor equipment is amazing

"bleeding edge": unforeseen, unknown, uncertain = normal

failing late = very costly

failing early = learning very fast

## *lessons for other domains*

other domains with increasing innovation rate (decreasing time-to-market) will get more unforeseen, unknown, uncertain issues

failing early is always better than failing late

Early *investments* in

test rigs, prototypes, virtual models, and simulations

*save* a lot of money